# VARIABLE CAPACITOR FOR TUNED CIRCUITS

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## CROSS-REFERENCE TO RELATED APPLICATIONS

**[0001]** This application claims priority, under 35 U.S.C. §119(e), of provisional application No. 60/226,179, filed August 18, 2000.

## STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

**[0002]** Not applicable.

## BACKGROUND OF THE INVENTION

**[0003]** This invention is in the field of integrated circuits, and is more specifically directed to variable capacitor circuits.

**[0004]** As well known in the art, variable capacitors are useful circuit elements in many applications. Communications systems, particularly those involving the generation and receipt of periodic signals, such as modulated radio signals, often involve the controlled tuning of circuits to particular frequencies. Variable capacitors are of course useful in such tuning. With the extremely high frequencies involved in modern communications, such frequencies ranging up to on the order of GHz, and also considering the narrow subchannels often used in broadband communications, the requirements for tuning accuracy and stability over temperature have become quite stringent.

**[0005]** Of course, most modern communications systems include tuning circuits that are realized in integrated circuits. Conventional variable capacitors in integrated

circuits are realized as either bipolar or metal-oxide-semiconductor (MOS) varactors. These conventional varactors have to date been limited in their quality factor, narrow capacitance ratios ($C_{max}/C_{min}$), and significant temperature sensitivity. The capacitance of conventional MOS varactors also varies over time. Accordingly, conventional varactors for integrated circuits are not well-suited for the high demands of precision and stability desired for modern high-frequency communications systems such as wireless handsets.

**[0006]** According to another conventional approach, tuning circuits are implemented by way of an array of switched fixed capacitors. Typically, the array includes binary-weighted switched capacitors, with the overall capacitance of the array determined by a digital word that controls the interconnection of the capacitors. The interconnection among the binary-weighted capacitors is effected by switches, such as MOS transistors, that are controlled in response to the digital control word.

**[0007]** By way of background, attention is directed to Figure 1 for a description of a well-known switched variable capacitor. According to this arrangement, two capacitors $2_A$, $2_B$ are connected in series between terminals A, B, by way of transistor 4, which serves as a switch. In this example, transistor 4 is an enhancement-mode n-channel MOS transistor, connected as a pass gate. As such, capacitors $2_A$, $2_B$ are connected to respective source/drain regions of transistor 4. A switching signal is applied to terminal SW and thus to the gate of transistor 4, selectively turning transistor 4 on and off, and thus selectively connecting and disconnecting capacitors $2_A$, $2_B$. The network of Figure 1 therefore provides a variable capacitance, in that it can selectably provide, between terminals A, B, a maximum capacitance $C_{max}$ and a minimum capacitance $C_{min}$. In this example, maximum capacitance $C_{max}$ is presented with transistor 4 on, and minimum capacitance $C_{min}$ is presented with transistor 4 off.

**[0008]** Figure 2a schematically illustrates the maximum capacitance case in which transistor 4 is on, connecting capacitors $2_A$, $2_B$ in series as shown. The maximum capacitance $C_{max}$ between terminals A, B is thus simply the series capacitance:



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$$C_{max} = \frac{C_A C_B}{C_A + C_B}$$

or, in the case where $C_A=C_B=C$:

$$C_{max} = \frac{C}{2}$$

**[0009]** Figure 2b schematically illustrates the minimum capacitance case in which transistor 4 is off, disconnecting the capacitors $2_A$, $2_B$ from one another, at least in the direct sense. As noted above, however, in this example, capacitors $2_A$, $2_B$ each have a plate connected to a source/drain region of transistor 4. This connection gives rise to parasitic junction capacitances $C_{jA}$, $C_{jB}$, respectively, which couple capacitors $2_A$, $2_B$ to ground, as shown in Figure 2b, and thus to one another. Another source of parasitic capacitance is bottom capacitance $C_{bA}$, $C_{bB}$ between the capacitor bottom plate and the underlying substrate. The overall parasitic capacitance Cp for each capacitor 2 is the sum $C_p = C_j + C_b$; in this conventional arrangement, however, junction capacitance $C_j$ is much larger than the bottom capacitance $C_b$. Assume, for the sake of description, that $C_A=C_B=C$ and that $C_{pA}=C_{pB}=C_P$. Considering these parasitic capacitances $C_{pA}$, $C_{pB}$, the minimum capacitance between terminals A, B, in the network of Figure 1 is:

$$C_{min} = \frac{CC_p}{2(C + C_p)}$$

**[0010]** Particularly in constructing a binary-weighted array of switched capacitors, for use in a tuning circuit, the range of each switched capacitor is an important parameter. For the variable capacitance network of Figure 1, this range corresponds to the ratio $C_{max}/C_{min}$, which (for $C_A=C_B=C$ and that $C_{pA}=C_{pB}=C_P$) is:

$$\frac{C_{max}}{C_{min}} = \frac{\frac{C}{2}}{\frac{CC_p}{2(C + C_p)}} = \frac{C + C_p}{C_p}$$

Accordingly, if the parasitic capacitance $C_p$ is minimized, the range of the switched variable capacitor will be high.

**[0011]** However, another important parameter in switched capacitor networks, particularly those intended for use at high frequencies such as encountered in wireless communications, is the quality factor, or Q, of the capacitors. To obtain a high quality factor, the on resistance of transistor 4 should be as small as possible, which is accomplished by increasing the channel width/length ratio of the device. However, as the junction width increases, the parasitic junction capacitance $C_p$ also increases, decreasing the tuning ratio $C_{max}/C_{min}$. A tradeoff between quality factor and capacitance range results.

**[0012]** Another limitation of this conventional switched variable capacitor is the difficulty of properly biasing switching transistor 4. According to conventional arrangements, such as shown in Figure 1, only the gate voltage (terminal SW) is controlled; no external bias is typically applied to the source/drain regions. This lack of bias can result in uncertainty of the state of the capacitor, if the source/drain regions float. In addition, because junction capacitance varies with the voltage across the junction, and because the parasitic junction capacitance is such an important factor in the performance of the network, it would be desirable to bias these junctions in such a manner as to minimize the parasitic capacitance $C_p$ when transistor 4 is off. To preserve a reasonable quality factor for the case with transistor 4 is off, however, the bias of the source/drain junctions should be provided through resistors that are as large as possible. Such large bias resistors will not only occupy significant chip area, particularly in the fabrication of an array of switched capacitors, but may also introduce noise into the network, which is especially undesirable in high-frequency applications.

## BRIEF SUMMARY OF THE INVENTION

**[0013]** It is therefore an object of the present invention to provide a switched capacitor with a large maximum-to-minimum capacitance ratio, for use in a variable capacitor network.

**[0014]** It is a further object of the present invention to provide such a switched capacitor in which bias is provided to source and drain regions of the switching transistor, without adversely affecting the quality factor of the device, and without requiring large chip areas.

**[0015]** It is a further object of the present invention to provide such a switched capacitor that is especially well-suited for high-frequency applications, such as wireless broadband communications.

**[0016]** It is a further object of this invention to provide such a switched capacitor that is stable over temperature.

**[0017]** It is a further object of this invention to provide such a switched capacitor that is biased to have a maximum Q in its maximum capacitance state.

**[0018]** It is a further object of this invention to provide such a switched capacitor that is suitable for digital control, thus avoiding the necessity for precise analog control voltages.

**[0019]** Other objects and advantages of the present invention will be apparent to those of ordinary skill in the art having reference to the following specification together with its drawings.

**[0020]** The present invention may be implemented into a switched capacitor network, for selectively connecting or disconnecting two capacitors in series with one another. A switch field-effect transistor is provided in series with the capacitors. Two bias transistors are connected to each side of the switch transistor, to bias the source and



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drain of the switch transistor to a reference voltage when the switch capacitor is on. A pair of complementary bias transistors are also connected to each side of the switch transistor, to bias the source and drain of the switch transistor to a selected bias voltage, different from the reference voltage, when the switch capacitor is off. Junction parasitic capacitance at the switch device is minimized.

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## BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

**[0021]** Figure 1 is an electrical diagram, in schematic form, of a conventional switched variable capacitor.

**[0022]** Figures 2a and 2b are electrical diagrams, in schematic form, of the conventional network of Figure 1 in its on and off states, respectively.

**[0023]** Figure 3 is an electrical diagram, in schematic form, of a switched variable capacitor according to the preferred embodiment of the invention.

**[0024]** Figure 4 is an electrical diagram, in schematic form, of a switched variable capacitor array according to the preferred embodiment of the invention.

**[0025]** Figure 5 is an electrical diagram, in block form, of a voltage controlled oscillator according to the preferred embodiment of the invention.

## DETAILED DESCRIPTION OF THE INVENTION

**[0026]** The present invention may be implemented in any circuit application in which a variable capacitor may be used, particularly a digitally controlled switched variable capacitor. An important application for variable capacitors are tuning circuits, in which the operation of a circuit is to be matched to a selected frequency by varying a capacitance in the circuit.

**[0027]** In particular, the present invention is believed to be especially well-suited for use in connection with high-frequency, high-performance, phase-locked loops as used in the modulation of radio frequency communications signals in wireless telephone handsets. As is known in that art, high-frequency phase-locked loops are useful in producing stable modulated signals, such as frequency-shift-keyed (FSK) modulated signals. A fundamental building block in such phase-locked loops is the voltage-controlled oscillator (VCO), which generates a periodic signal at a frequency controlled by an error signal from a phase-frequency detector; this error signal corresponds to the difference between a reference clock and a feedback signal derived from the phase-locked loop output in combination with the signal to be communicated. A variable capacitance can be used in the VCO to control the frequency of its oscillation. It is contemplated that a binary-weighted array of switched variable capacitors constructed according to this invention will be especially beneficial when used as a variable capacitor in such high-performance VCOs and phase-locked loops. An example of such an application of the switched variable capacitor according to this invention will be described below.

**[0028]** Alternatively, this invention may be used in connection with variable capacitors in a wide range of applications. It is contemplated that those skilled in the art having reference to this specification will be readily able to implement this invention in such circuits and applications. It is therefore to be understood that the following description is provided by way of example only, and is not meant to limit the true scope of the invention as claimed.

[0029] Referring now to Figure 3, variable capacitor 20 according to the preferred embodiment of the invention includes capacitors $12_A$, $12_B$, connected to terminals A, B, respectively. Each of capacitors 12 may be constructed in the conventional manner for integrated circuit capacitors, examples of which include polysilicon-to-polysilicon thin film capacitors, polysilicon-to-diffusion capacitors, and the like. However, for purposes of temperature stability of capacitor 20 over temperature, capacitors 12 are preferably metal-to-metal capacitors.

[0030] Each of capacitors $12_A$, $12_B$ are also connected to a source/drain region of transistor 14. As such, as shown in Figure 3, switched variable capacitor 20 includes the series connection of capacitor $12_A$, transistor 14, and capacitor $12_B$ between terminals A and B. The gate of transistor 14 receives a control signal from terminal SW. In this embodiment of the invention, transistor 14 is an n-channel enhancement-mode MOS transistor. In order to maximize the quality factor of variable capacitor 20, transistor 14 is preferably a relatively large device in terms of drive capability, having a relatively large channel width-to-length ratio (e.g., on the order of 20 or greater) so that its on-resistance is minimized. Transistor 14 may also be realized by way of two or more MOS transistors connected in parallel.

[0031] Bias transistors $16_A$, $16_B$ are provided in switched variable capacitor 20 according to the preferred embodiment of the invention. According to this embodiment of the invention, bias transistors 16 are also n-channel enhancement-mode MOS transistors, although preferably having the minimum channel width available for the manufacturing technology (for example, having a width/length ratio of on the order of 1.5). The drain of transistor $16_A$ is connected to the source/drain region of transistor 14 at the point at which it is connected to capacitor $12_A$, and the drain of transistor $16_B$ is connected to the source/drain region of transistor 14 at the point at which it is connected to capacitor $12_B$. The sources of transistors 16 are both connected to a reference voltage, such as ground, and the gates of transistors 16 are connected together and to terminal SW to receive the switching control signal. According to this embodiment of the invention, because bias transistors 16 and switching transistor 14 are both n-channel

devices, and have their gates connected in common, bias transistors 16 are turned on when transistor 14 is on, and off when transistor 14 is off. The bias to ground provided by transistors 16 ensures that the on-resistance of transistor 14 is minimized, maximizing the Q for switched variable capacitor 20 in its maximum capacitance state.

[0032] Switched variable capacitor 20 according to this embodiment of the invention also includes bias transistors $18_A$, $18_B$ for biasing the source/drain regions of transistor 14 when the device is off. In this preferred embodiment of the invention, bias transistors $18_A$, $18_B$ are p-channel enhancement-mode MOS transistors, preferably of minimum channel width (for example, having a width-to-length ratio of on the order of two). The source of transistor $18_A$ is connected to the source/drain region of transistor 14 at the point connected to capacitor $12_A$, and the source of transistor $18_B$ is connected to the source/drain region of transistor 14 at the point connected to capacitor $12_B$. The gates of transistors $18_A$, $18_B$ are connected together, and to terminal SW to receive the switching control signal. The drains of transistors $18_A$, $18_B$ are connected together, and are biased to bias voltage $V_P$.

[0033] Because, in this example, transistors 18 are p-channel while transistors 14, 16 are n-channel, transistors 18 are on when transistors 14, 16 are off, and transistors 18 are off when transistors 14, 16 are on. Alternatively, if transistors 14, 16, 18 are all of the same conductivity type, this complementary arrangement may be implemented by applying the logical complement of the signal at terminal SW to the gates of transistors 18. In either case, transistors 18 bias the source/drain regions of transistor 14 from bias voltage $V_P$ when transistor 14 is off. As will be described below, bias voltage $V_P$ is preferably selected to be at a relatively high voltage (near the $V_{cc}$ power supply in this example), to minimize parasitic capacitance.

[0034] In operation, the state of switched variable capacitor 20 is set by the logic level at terminal SW. In this example, the maximum capacitance state is selected by terminal SW being driven to a high logic level. This turns on transistors 14, $16_A$, $16_B$, and turns off transistors $18_A$, $18_B$. With transistor 14 turned on, capacitors $12_A$, $12_B$ are

connected to one another, presenting the maximum capacitance $C_{max}$ between terminals A and B. Generally, where capacitors $12_A$, $12_B$ have capacitances $C_A$, $C_B$, maximum capacitance $C_{max}$ will be:

$$C_{max} = \frac{C_A C_B}{C_A + C_B}$$

or, in the special case of $C_A$=$C_B$=C:

$$C_{max} = \frac{C}{2}$$

The source/drain regions of transistor 14 will be biased by transistors 16 toward ground. The effects of this bias by transistors 16 are to maintain the source/drain nodes of transistor 14 from floating, and to minimize the on-resistance of transistor 14, as noted above.

**[0035]** Conversely, in this example, a low logic level at terminal SW will turn off transistor 14, opening the direct connection between capacitors $12_A$, $12_B$. In addition, bias transistors 16 are turned off, and bias transistors $18_A$, $18_B$ are turned on. This state of switched variable capacitor 20 presents the minimum capacitance $C_{min}$ between terminals A, B, and biases the source/drain regions of off-state transistor 14 to voltage $V_P$. According to this embodiment of the invention, for example in the case where $C_A$=$C_B$=C, and where capacitors $12_A$, $12_B$ each have a parasitic capacitance $C_p'$, minimum capacitance $C_{min}$ can be evaluated as:

$$C_{min} = \frac{CC_p'}{2(C + C_p')}$$

Parasitic capacitance $C_p'$ depends upon the voltage $V_P$, as will now be discussed.

**[0036]** As described above, in this embodiment of the invention, the parasitic capacitance $C_p'$ for each of capacitors $12_A$, $12_B$ is the sum of its junction capacitance $C_j$ at the junction between each of the source/drain regions of transistor 14 and the underlying substrate or well, plus the bottom capacitance $C_b$ between the capacitor

bottom plate and the integrated circuit substrate. For a reverse-biased p-n junction, the junction capacitance $C_j$ decreases with increases in the reverse bias voltage $V_R$ across the junction:

$$C_j \propto \frac{1}{\sqrt{V_R + V_{bi}}}$$

where $V_{bi}$ is the built-in voltage across the junction. As evident from this expression, the reverse bias voltage $V_R$ increases, the junction capacitance $C_j$ decreases; this relationship is due to the increase of the space-charge region at the reverse-biased junction with increasing reverse bias. For an n-channel device such as transistor 14, the junction capacitance is reduced with a positive voltage applied to the n-type source/drain regions. According to the preferred embodiment of the invention, therefore, bias voltage $V_P$ is preferably as high a voltage as available, for example at the $V_{cc}$ power supply to the integrated circuit embodying switched variable capacitor 20.

[0037] Bias transistors $18_A$, $18_B$ thus provide the important benefit of minimizing the parasitic junction capacitance $C_j$, and thus reducing the parasitic capacitance $C_p'$ that is presented to each of capacitors 12 in switched variable capacitor 20, by providing the optimal junction bias to the source/drain regions of transistor 14, when in the off-state. Additionally, by implementing bias transistors 18 to have as small a channel width/length ratio as possible, resulting in a relatively high on-resistance through transistors 18, the quality factor Q of switched variable capacitor 20 is degraded as little as possible.

[0038] A reduction in junction capacitance $C_j$ is of course reflected in a reduction in the parasitic capacitance $C_p'$ presented to capacitors 12 when switching transistor 14 is off. Recalling that, for the case of $C_A$=$C_B$=C, the ratio of maximum capacitance $C_{max}/C_{min}$ is:

$$\frac{C_{max}}{C_{min}} = \frac{C + C_p^{'}}{C_p^{'}}$$

a reduction in the parasitic capacitance $C_p'$ will result in a geometric increase in the ratio $C_{max}/C_{min}$. An increase in this ratio provides important benefits in the implementation of switched variable capacitor 20 into an array, as the range and resolution of the switched capacitor array improves with increases in this ratio.

**[0039]** In addition, it is contemplated that the temperature stability of switched variable capacitor 20, particularly in its minimum capacitance state (transistor 14 off) is greatly improved by this invention. The relation of junction capacitance $C_j$:

$$C_j \propto \frac{1}{\sqrt{V_R + V_{bi}}}$$

indicates that as reverse bias voltage $V_R$ increases, the dependence of junction capacitance $C_j$ on the built-in voltage $V_{bi}$ decreases. The built-in voltage $V_{bi}$ is dependent on temperature, while the reverse bias voltage $V_R$ applied by bias transistors 18 can be regulated (by an on-chip voltage regulator, band-gap reference circuit, or the like) to be stable with temperature. As a result, an increase in the reverse bias voltage $V_R$ can reduce the temperature sensitivity of junction capacitance $C_j$. Because bias transistors 18 can apply a stable, high magnitude, reverse bias voltage $V_R$ across the source/drain junctions of transistor 14, the junction capacitance $C_j$ can therefore be made significantly more stable over temperature than according to conventional circuits. Stability of parasitic capacitance $C_p'$ over temperature thus translates into temperature stability of the minimum capacitance $C_{min}$, which depends on parasitic capacitance $C_p'$:

$$C_{min} = \frac{CC_p'}{2(C + C_p')}$$

The capacitance of switched variable capacitor 20 in the minimum capacitance state (transistor 14 off) is therefore rendered more stable by the present invention.

**[0040]** Of course, the capacitance of switched variable capacitor 20 in the maximum capacitance state is dependent almost exclusively on the capacitance of each of capacitors 12. According to this invention, the temperature stability of this

capacitance is optimized by implementing capacitors 12 as metal-to-metal capacitors, as these devices exhibit extremely low temperature coefficients (e.g., on the order of 10 ppm/°C.).

**[0041]** According to this invention, therefore, a switched variable capacitor is provided that is suitable for use in high-frequency, high performance, applications such as may be used in modern communications systems and devices. For example, it is contemplated that this invention can provide a switched variable capacitor having a high quality factor Q, for example greater than 30, at frequencies on the order of 2.5 GHz, with a tuning range, or capacitance ratio $C_{max}/C_{min}$, of greater than two.

**[0042]** Referring now to Figure 4, an exemplary implementation of switched variable capacitor 20 into binary-weighted capacitor array 40 will now be described. As noted above, switched variable capacitor 20 is well-suited for implementation into a digitally controlled array 40, to provide a variable capacitance useful in tuning digital circuits and systems. According to this embodiment of the invention, array 40 arranges switched variable capacitors 20, all of a unit maximum capacitance $C_{max}$, and thus with all capacitors 20 (including both the capacitors 12 and the transistors 14, 16, 18) of identical size, into an array. Such unit sizing can result in an efficient circuit layout.

**[0043]** Binary weighted array 40 of Figure 4 presents a variable capacitance between terminals A, B, with the capacitance varying according to the digital value on control lines SW. In this example, control lines SW[0:3] present four digital bits, ranging from least significant bit SW[0] to most significant bit SW[3]. Accordingly, a single unit capacitance presented by a single switched variable capacitor 20 as described above is connected between terminals A, B, and is controlled by least significant control bit SW[0] (and corresponds to variable capacitance $30_0$). Variable capacitance $30_1$ includes two switched variable capacitors 20, both of unit size and thus identical to capacitor 20 in capacitance $30_0$, connected in parallel between terminals A, B, and both controlled by control bit SW[1]. Accordingly, variable capacitance $30_1$ has a maximum capacitance that is twice that of variable capacitance $30_0$; control line SW[1] thus has twice the weight



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of control line SW[0]. Similarly, the next most significant control bit SW[2] controls variable capacitance $30_2$, which includes four switched variable capacitors 20, all of unit capacitance and connected in parallel between terminals A, B. In this four-bit example, most significant control line SW[3] controls variable capacitance $30_3$, which consists of eight switched variable capacitors 20, of unit capacitance, connected in parallel between terminals A, B.

**[0044]** In operation, the value of capacitance presented by array 40 between terminals A, B is controlled by the digital value on the four bits of control lines SW[0:3]. Each of variable capacitances 30 for which its associated control line SW is low, in this example, presents a capacitance corresponding to the minimum capacitance $C_{min}$ of switched variable capacitor 20, times the number of capacitors 20 in its stage; conversely, each of variable capacitances 30 receiving a high level on its associated control line SW presents a capacitance between terminals A, B corresponding to the maximum capacitance $C_{max}$ of its switched variable capacitors 20, times the number of capacitors 20 in that stage. Accordingly, binary weighted array 40 according to this embodiment of the invention provides a digitally controlled variable capacitance that has a sizable dynamic range. Additionally, the time and temperature stability discussed above for an individual capacitor 20 is achieved by array 40 on this larger scale. The unit capacitor implementation of array 20 is also conducive to efficient chip layout.

**[0045]** As noted above, binary-weighted array 40 of switched variable capacitor 20 according to the present invention is particularly useful in connection with high-frequency, high performance, circuit applications. One example of such an application is a voltage controlled oscillator (VCO). Referring now to Figure 5, VCO 50 constructed according to the preferred embodiment of the invention will now be described, by way of example.

**[0046]** In this example, VCO 50 is a digitally-controlled oscillator that generates a periodic signal across its terminals VON, VOP, at a frequency controlled by the value of the digital word presented on control lines SW[0:n]. For the example in which VCO

50 is implemented in a phase-locked loop, this digital word corresponds to the output from a phase-frequency detector. This output is an error signal based upon a comparison of a feedback signal from VCO 50 itself (divided down in frequency if desired) to a reference clock signal. In this case, VCO 50 is controlled by the digital word corresponding to this error signal to modulate its output in a direction that brings the feedback signal closer to a match with the reference clock. Of course, VCO 50 may be used in other applications besides phase-locked loops, such other applications including signal generators, tuning circuits, and the like.

**[0047]** VCO 50 of Figure 5 is arranged as a conventional L-C CMOS oscillator, with the frequency of oscillation determined by binary weighted array 40, under the control of control lines SW. Current source 41 is coupled between the $V_{cc}$ power supply and the sources of cross-coupled p-channel transistors $42_0$, $42_1$. The drain of transistor $42_0$ is connected to output terminal VON and to the gate of transistor $42_1$, while the drain of transistor $42_1$ is connected to output terminal VOP and to the gate of transistor $42_0$. N-channel transistors $44_0$, $44_1$ have their drains connected to terminals VON, VOP, respectively, have their sources biased to ground, and have their gates cross-coupled (the gate of transistor $44_0$ is connected to the drain of transistor $44_1$, and the gate of transistor $44_1$ is connected to the gate of transistor $44_0$). The oscillator is completed by inductor 44 and binary-weighted array 40, constructed as described above relative to Figure 4, connected in parallel with one another between terminals VON, VOP.

**[0048]** In operation, the current sourced by current source 41 is conducted alternately by the legs of VCO 50, in the manner well-known for conventional cross-coupled oscillators. The frequency of oscillation is determined by the inductance of inductor 44, which is fixed in this example, and the capacitance presented by binary-weighted capacitor array 40 responsive to the digital control word on lines SW[0:n]. As conventional in the art, the higher the capacitance presented by array 40, the lower the frequency of oscillation, and vice versa.

[0049] As noted above, the dynamic range presented by binary-weighted array 40 of switched variable capacitors 20 provides for a wide tuning range of VCO 50 of Figure 5. In addition, precise digital control is provided by array 40, particularly when realized by unit capacitances as described above relative to Figure 4. Also as noted above, switched variable capacitors 20 provide excellent stability over temperature, and over time as array 40 is cycled. These benefits are especially important in precision circuits such as VCO 50, making this circuit suitable for excellent performance in such applications as transmission signal modulation in wireless handsets and the like.

[0050] Of course, the present invention may also be implemented, and its benefits obtained, in a wide range of tuning and tunable circuits, and in any application in which a precision variable capacitor is useful.

[0051] While the present invention has been described according to its preferred embodiments, it is of course contemplated that modifications of, and alternatives to, these embodiments, such modifications and alternatives obtaining the advantages and benefits of this invention, will be apparent to those of ordinary skill in the art having reference to this specification and its drawings. It is contemplated that such modifications and alternatives are within the scope of this invention as subsequently claimed herein.

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